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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/735,517

12/11/2003

Gernot Eckstein

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EXAMINER

JOHNSON, CARLTON

ART UNIT

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2436

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/735,517	Applicant(s) ECKSTEIN ET AL.	
	Examiner CARLTON V. JOHNSON	Art Unit 2436	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10-8-2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3 and 5-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3 and 5-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This action is in response to application amendments filed on 10-8-2009.
2. Claims **1, 3, 5 - 10** are pending. Claim **1** has been amended. Claims **2, 4** have been cancelled. Claims **1, 3** are independent. This application was filed on 12-11-2003.

Response to Remarks

3. Applicant's arguments have thus been fully considered but they were not persuasive.

- 3.1 Applicant argues that the referenced prior art does not disclose, voltage variation using the random number generator.

Schulz discloses: "The frequency of the voltage variation is random and is produced by noise on the power supply and supply lines itself, and is also produced by on-chip noise sources 40' which include the switching of other circuits on the same semiconductor chip. "

The voltage variation can be caused by the switching or operation of a circuit on the semiconductor chip. The generation of random numbers results in the operation of a circuit on the chip. Its operation results in the generation of noise and an additional adjustment in the varying of noise and therefore the varying of voltage. (Schultz col. 6, line 41 - col. 7, line 23)

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, **3, 5, 7 - 10** are rejected under 35 U.S.C. 103(a) as being anticipated over **Schulz et al.** (US patent No. **4,905,176**).

With Regards to Claim 1, Schulz discloses a method of preventing the external detection of operations in a digital integrated circuit (Schulz col. 5, lines 67 - col 6, line 1: position circuit on an integrated circuit chip) comprising an asynchronous circuit (Schulz col. 2, lines 27-31: asynchronous serial number output), comprising time-varying a supply voltage of said asynchronous circuit, by a random number generator, to time-shift the execution time of operations within said asynchronous circuit; wherein the time variation of said supply voltage takes place in a random way. (Schulz col. 2, lines 47-54: time varying power supply voltage; frequency of operation causes a non-periodic serial random number sequence; col. 8, line 65 -col. 9, line 40 disclosing power supply voltage randomly varies with time and applying delay (time-shift) due to the randomly varying supply voltage; col. x, lines x:)

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With Regards to Claim 3, Schulz discloses a digital integrated circuit comprising: an asynchronous circuit (Schulz col. 2, lines 27-31: asynchronous serial number output), and means for time-varying a supply voltage of said asynchronous circuit to time-shift the execution point of operations within said asynchronous circuit, wherein said means for time-varying said supply voltage comprising a random number generator. (see Schulz col. 2, lines 47-54: frequency of operation; random number generator causes a non-periodic serial random number sequence to be produced; col. 8, line 65 -col. 9, line 40 disclosing power supply voltage randomly varies with time and applying delay (time-shift) due to the randomly varying supply voltage)

With Regards to Claim 5, Schulz discloses the digital integrated circuit according to claim 3, wherein said means for time-varying said supply voltage comprises a noise voltage source driving said random-number generator. (see Schulz col. 4, lines 30-36: frequency of voltage variation is produced by noises on the power supply or supply lines)

With Regards to Claim 7, Schulz discloses the digital integrated circuit according to claim 3, wherein said means for time-varying said supply voltage further comprises a voltage regulator. (see Schulz col 2, lines 47-54: varying or regulating (regulator) power supply voltages)

With Regards to Claim 8, Schulz discloses the digital integrated circuit according to

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claim 3, wherein said asynchronous circuit is formed for executing a coding algorithm.

(see Schulz col. 8, lines 51-58: finds application in cryptography; creation of master key values used for cryptographic operations)

With Regards to Claims 9, 10, Schulz discloses the method, digital integrated circuit according to claims 1 and 3, wherein the asynchronous circuit is a type, which performs processing without correlation to a clock. (see Schulz col. 4, lines 30-36: frequency of voltage variation is produced by noise on power supply and supply lines itself)

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim **6** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Schulz** and further in view of **Read et al.** (US Patent No. **5,353,243**).

With Regards to Claim 6, Schulz discloses the digital integrated circuit according to claim 4, wherein said means for time-varying said supply voltage further comprising a random-number generator. (Schulz col. 2, lines 47-54: time varying power supply voltages; pseudo-random number generator causes a non-periodic serial random

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number sequence to be produced)

Niessen does not specifically disclose a digital-analog converter transforming the digital values into an analog voltage. However, Read discloses wherein a digital-analog converter transforming the digital values into an analog voltage. (see Read col. 25, lines 29-31: reference voltages are supplied by a digital to analog converter)

It would have been obvious to one of ordinary skill in the art to modify Niessen for a digital-analog converter transforming the digital values into an analog voltage as taught by Read. One of ordinary skill in the art would have been motivated to employ the teachings of Read for systems used by electronics designers to simulate the operation of electronic circuits during development and testing of electronic systems including circuits to combat attacks on integrated circuits. (see Read col. 1, lines 11-10)

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carlton V. Johnson whose telephone number is 571-270-1032. The examiner can normally be reached on Monday thru Friday , 8:00 - 5:00PM EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami can be reached on 571-272-4195. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nasser Moazzami/
Supervisory Patent Examiner, Art Unit 2436

Carlton V. Johnson
Examiner
Art Unit 2436

CVJ
January 4, 2010